CLAIMS

1. A bus comprising:

a master interface configured to (i) receive an early command signal having a predetermined timing relationship to a first clock edge and (ii) present a bus wait signal proximate a second clock edge;

a slave interface configured to (i) present a command signal a delay after said first clock edge and (ii) receive a slave wait signal; and

a control logic configured to (i) register said early command signal to generate said command signal and (ii) convert said slave wait signal into said bus wait signal.

2. The bus according to claim 1, wherein (i) said master interface is further configured to receive an early address signal having said predetermined relationship with said first clock edge, (ii) said control logic is further configured to register said early address signal to generate an address signal and decode said address signal to generate a device select signal, and (iii) said slave interface is further configured to present said address

signal and said device select signal said delay after said first clock edge.

3. The bus according to claim 2, wherein (i) said master interface is further configured to receive a no-address signal having said predetermined relationship to said first clock signal and (ii) said control logic is further configured to inhibit said slave select signal in response to said no-address signal.

4. The bus according to claim 1, wherein (i) said master interface is further configured to receive an early burst request signal having said predetermined timing relationship to said first clock edge, (ii) said control logic is further configured to register said early burst request signal to generate a burst request signal, and (iii) said slave interface is further configured to present said burst request signal said delay after said first clock edge.

5. The bus according to claim 1, wherein (i) said master interface is further configured to receive a bus request signal and present a bus grant signal, and (ii) said control logic

is further configured to arbitrate in response to said bus request signal and generate said bus grant signal.

6. The bus according to claim 5, wherein said control logic is further configured to complete arbitration within one clock cycle and present said command signal in a next clock cycle.

7. The bus according to claim 5, wherein (i) said master interface is further configured to receive a lock signal, and (ii) said control logic is further configured to halt arbitration responsive to said lock signal.

8. The bus according to claim 1, wherein said control logic comprises an address decoder configured to generate a plurality of device select signals responsive to an address signal.

9. The bus according to claim 8, wherein said control logic further comprises a plurality of registers configured to register a plurality of early signals each having said predetermined relationship to said first clock edge to generate a plurality of signals said delay after said first clock edge.

10. The bus according to claim 9, wherein said control logic further comprises an arbitration logic configured to generate a bus grant signal.

11. The bus according to claim 10, wherein said control logic further comprises a first multiplexer configured to multiplex said early signals responsive to said bus grant signal.

12. The bus according to claim 11, wherein said control logic further comprises a second multiplexer configured to select a write data select signal responsive to said bus grant signal.

13. A method for operating a bus comprising the steps of:

(A) receiving an early command signal having a predetermined timing relationship to a first clock edge at a master interface;

(B) registering said early command signal to generate a command signal in response to step (A);

(C) presenting said command signal a delay after said first clock edge at a slave interface in response to step (C);

(D) receiving a slave wait signal at said slave interface;

(E) converting said slave wait signal into a bus wait signal in response to step (D); and

(F) presenting said bus wait signal at said master interface proximate a second clock edge in response to step (E).

14. The method according to claim 13, further comprising the steps of:

receiving an early address signal having said predetermined relationship with said first clock edge at said master interface;

registering said early address signal in response to said first clock edge to generate an address signal;

presenting said address signal at said slave interface said delay after said first clock edge;

decoding said address signal to generate a device select signal in response to generating said address signal; and

presenting said device select signal at said slave interface in response to decoding said address signal.

15. The method according to claim 14, further comprising the steps of:

receiving a no-address signal having said predetermined timing relationship to said first clock edge at said master interface; and

inhibiting said early device select signal in response to receiving said no-address signal.

16. The method according to claim 13, further comprising the steps of:

receiving an early burst request signal having said predetermined timing relationship to said first clock edge at said master interface;

registering said early burst request signal to generate a burst request signal in response to said first clock edge; and

presenting said burst request signal at said slave interface said delay after said first clock edge.

17. The method according to claim 13, further comprising the steps of:

receiving a bus request signal at said master interface;

arbitrating in response to receiving said bus request signal; and

generating a bus grant signal at said master interface in response to arbitrating.

18. The method according to claim 17, wherein arbitrating is completed within one clock cycle and said command signal is presented in a next clock cycle.

19. The method according to claim 17, further comprising the steps of:

receiving a lock signal at said master interface in response to generating said bus grant signal; and

halting arbitration in response to receiving said lock signal.

20. A bus comprising:

means for receiving an early command signal having a predetermined timing relationship to a first clock edge at a master interface;

means for registering said early command signal to generate a command signal;

means for presenting said command signal a delay after said first clock edge at a slave interface;

means for receiving a slave wait signal at said slave interface;

means for converting said slave wait signal into a bus wait signal; and

means for presenting said bus wait signal at said master interface proximate a second clock edge.